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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Number:	09/885,792
Filing Date:	06/20/2001
Applicant:	Basanth Jagannathan
Application Title:	**A NON-SELF-ALIGNED SiGe HETEROJUNCTION BIPOLAR TRANSISTOR**
Examiner:	Lattin, Christopher W.
Art Unit:	2812

DECLARATION UNDER 37 CFR 1.131

Commissioner of Patents
P.O. BOX 1450
Alexandria, VA 22313-1450
Sir:

Basanth Jagannathan, Shwu-Jen Jeng, Jeffrey B. Johnson, Robb A. Johnson, Louis D. Lanzerotti, Kenneth J. Stein, and Seshadri Subbanna, applicants in the above-identified patent application, declare as follows:

1) During a period of time prior to September 1, 2000, the 35 USC 102(e) date of US patent 6,410,975 to Racanelli, we worked as a team and conceived of and reduced to practice the invention disclosed and claimed in the above-referenced application.

2) Specific proof of our conception and reduction to practice is evidenced by the attached Exhibit A (Disclosure FIS8-2000-0337), which is a confidential invention disclosure form used within the assignee corporation, IBM. The exhibit was prepared in preparation of a patent application. The work associated with the attached exhibit was the basis for the patent application referenced above.

3) Exhibit A describes and illustrates the non-self aligned transistor and fabrication method of the present invention. Specifically, Figs. 1a-1j of Exhibit A illustrate the prior art (also illustrated in Figs. 1A-1J in the present specification). Figs. 2a-2i of Exhibit A

illustrate the method of the present invention, including steps of intrinsic base implant (Fig. 2g) and deposition of the nitride layer (Fig. 2d) that provides an implant mask over the emitter pedestal.

4) The discussion on page 6 of Exhibit A provides further evidence of conception and reduction to practice.

5) Exhibit A was last modified on June 27, 2000 (see the top of page 1). This Exhibit demonstrates both conception and reduction to practice of the invention prior to the filing date of the Racanelli reference (September 1, 2000).

6) We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful, false statements so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful, false statements may jeopardize the validity of the above-referenced application and any patent issuing thereon.

Date 9/2/2003 Basanth Jagannathan Basanth Jagannathan

Date Sept 2, 2003 Shwu-Jen Jeng Shwu-Jen Jeng

Date _____ Jeffrey B. Johnson _____

Date _____ Robb A. Johnson _____

Date _____ Louis D. Lanzerotti _____

Date 9-2-03 Kenneth J. Stein Kenneth J. Stein

Date 9/2/03 Seshadri Subbanna, Seshadri Subbanna

EXHIBIT A

Disclosure FIS8-2000-0337

Created By: Shwu-Jen Jeng **Created On:** 09/07/99 02:14:47 PM
Last Modified By: Hilda Heinlein **Last Modified On:** 06/27/2000 05:19:53 PM

*** IBM Confidential ***

Required fields are marked with the asterisk (*) and must be filled in to complete the form.

Summary

Status	Under Evaluation
Processing Location	FIS
Functional Area	ZZISA-Issac
Attorney/Patent Professional	Joseph Abate/Fishkill/IBM
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Submitted Date	06/27/2000 09:30:20 AM
Owning Division [redacted]	MD
PVT Score [redacted]	To calculate a PVT score, use the 'Calculate PVT' button.
Incentive Program	
Lab	
Technology Code	101NS

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Peter Smeys/Fishkill/IBM	
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FIS8-2000-0337 A Non-Self Aligned SiGe Heterojunction Bipolar Transistor (HBT) - continued

Response Due to IPAC - 07/27/2000

Main Idea

Title of disclosure (in English)

A Non-Self Aligned SiGe Heterojunction Bipolar Transistor (HBT)

Idea of disclosure

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.

Using a non-self aligned scheme to replace the emitter pedestal and self-aligned extrinsic base structure, the total process time and thermal cycle for the non-self aligned scheme will be reduced compared to the self-aligned structure. In the simplified process of forming the non-self aligned emitter, due to the reduced transient enhanced diffusion of the dopants much sharper and narrower doping profiles can be obtained. As a result, the transistor structure can be tailored for high-speed performance. The reduced process time also lowers the cost of fabricating the device.

A related advantage in this low thermal cycle processing is that it allows for making use of thin LTE layers to form base and collector regions. This leads to possibilities of even higher speed devices. The ability to integrate thin LTE layers in this structure also implies that the overall device topography can be lowered making MEOL processing much easier.

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?

After LTE in-situ boron doped base been put down, a conventional dielectric emitter pedestal and a self-aligned extrinsic base spacer structure as shown in Figure 1j will require additional pedestal RIE, spacer deposition and etch, oxide strip, high pressure oxidation, and emitter opening RIE process steps before reaching emitter poly deposition.(The film thickness scaled down by approximately 20% from generation 5HP to generation 7HP.)

Insert text description of ETX process (5 and 6HP) for Figures 1a-1j.

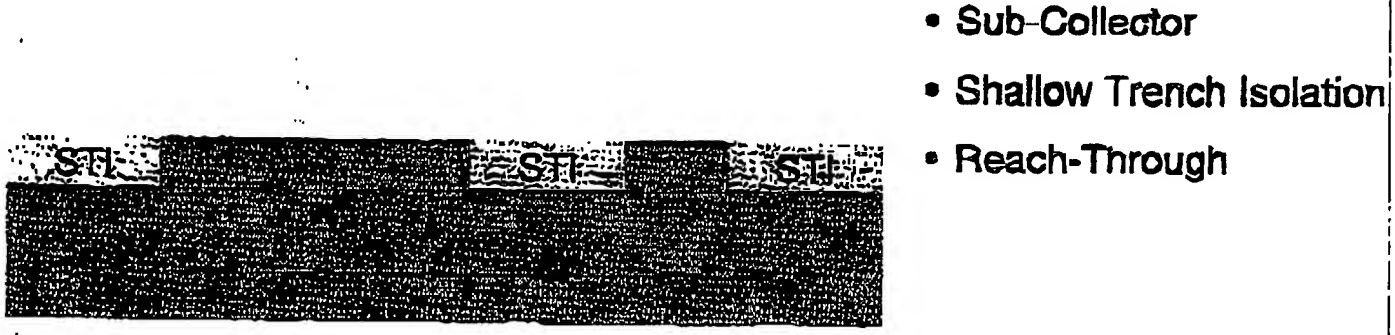


Figure 1a.

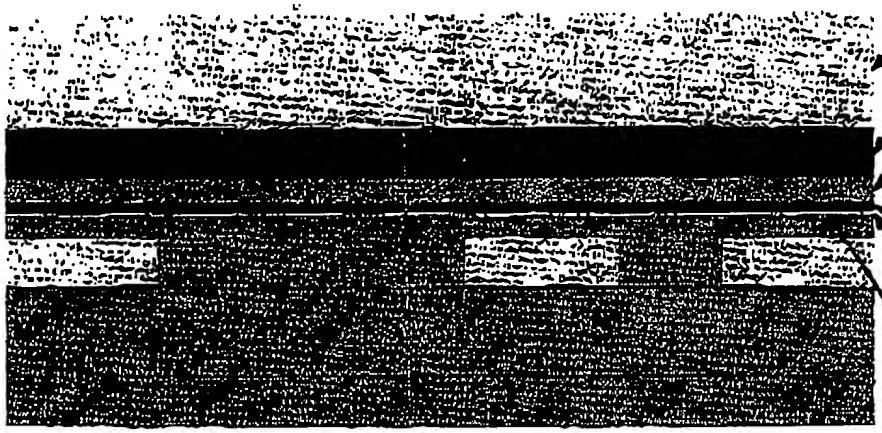


Figure 1b.

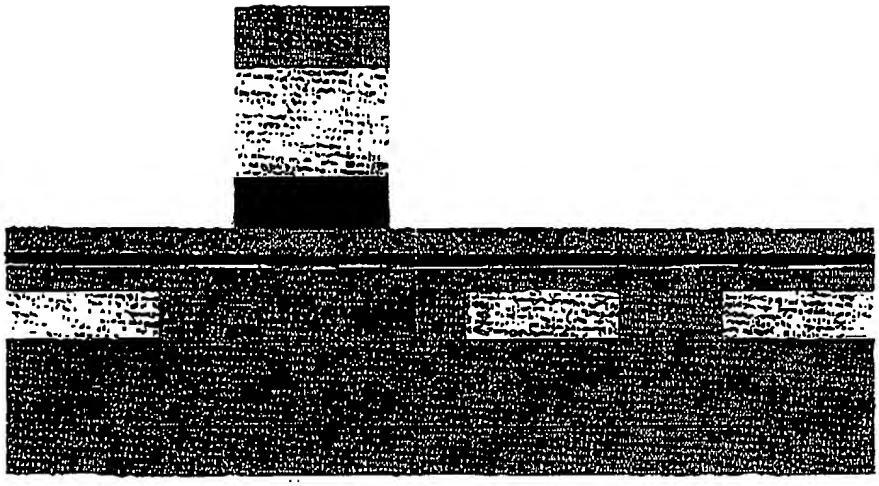


Figure 1c.

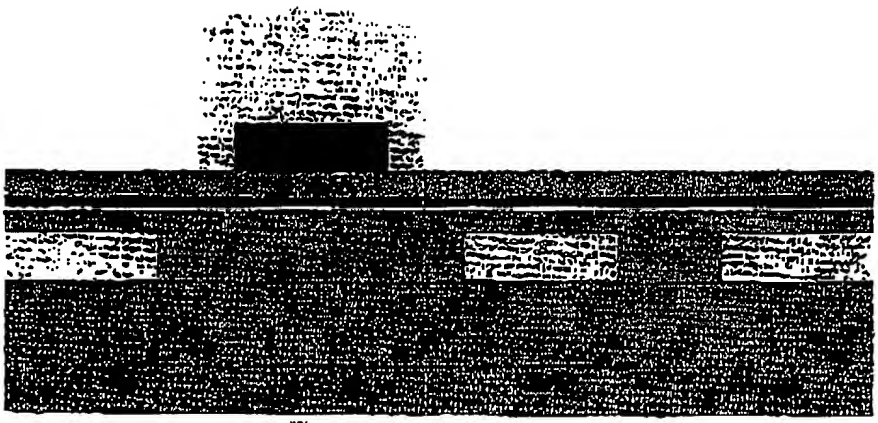


Figure 1d.

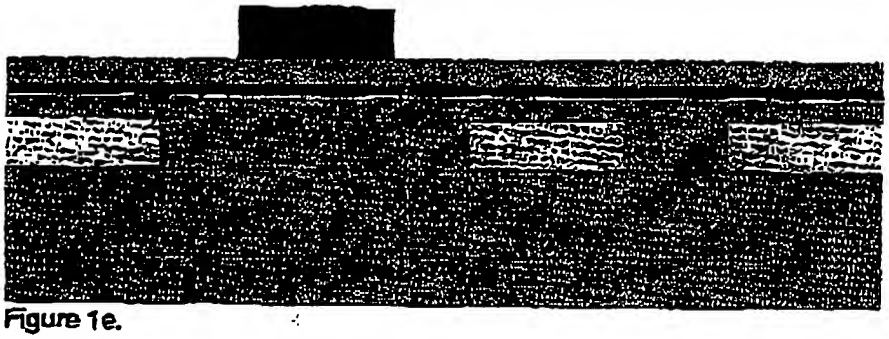


Figure 1e.

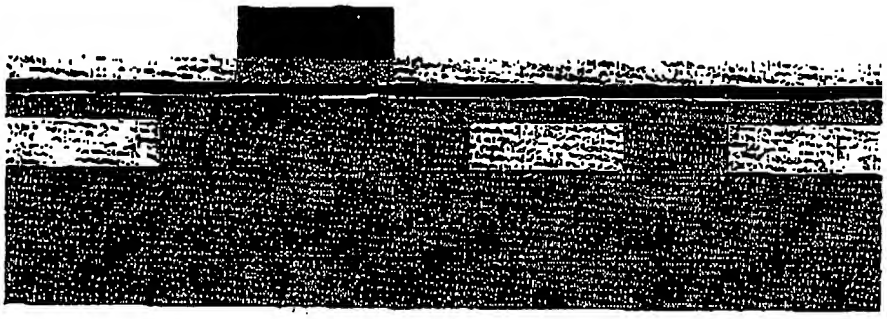


Figure 1f.

- Convert Polysilicon to Oxide
  - HiPOx

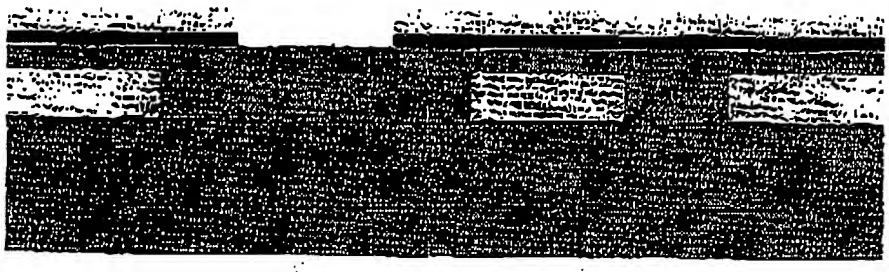
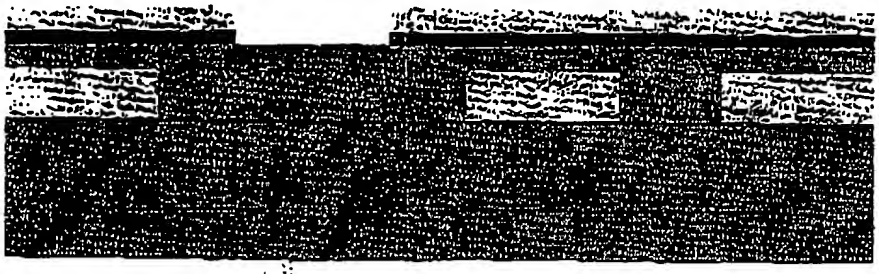


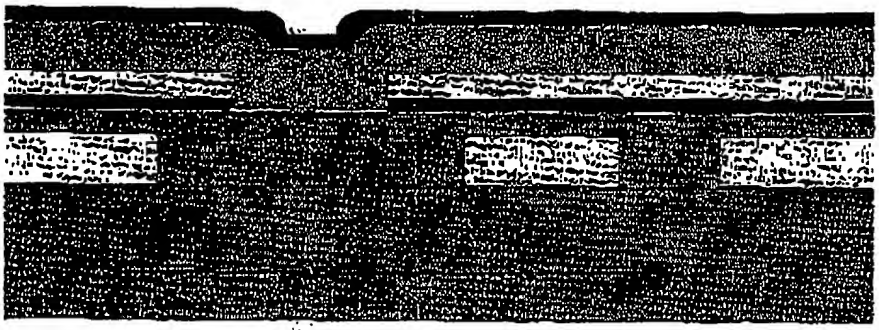
Figure 1g.

- Remove Nitride
- Remove Polysilicon
- Remove Nitride



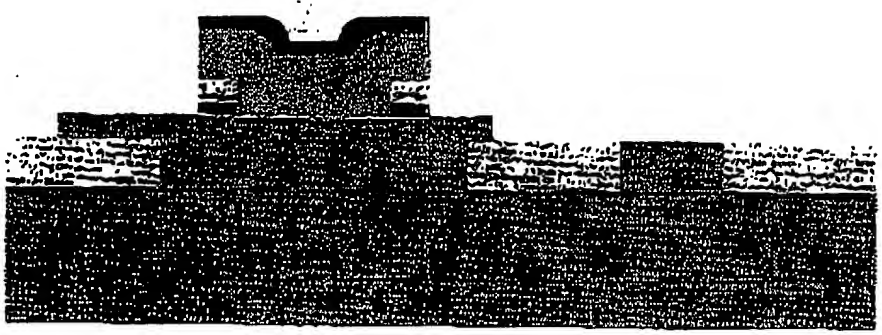
- Pedestal Implant for High f_t Device
  - Phosphorous
- Self-aligned to Extrinsic Base Implant

Figure 1h.



- Rapid Thermal Oxidation
- Emitter Polysilicon Deposition and Implant
  - Arsenic
- Protect Nitride
- Emitter RTA

Figure 1i.



- Emitter Photo and Etch
- Base Photo and Etch

Figure 1j.

As seen from the prior art the self-aligned process is complicated and time consuming. Using a non-self aligned structure, the complicated emitter pedestal is no longer needed. Instead, the emitter stack now consists of 100A HIPOx, 500A RTCVD nitride, and 700A LPVCD or PECVD TEOS as shown in Figure 2a. (The 500A RTCVD nitride can be replaced by an 600A PECVD nitride to further reduce thermal cycle. This 600A PECVD nitride will

be reduced to 500A after NP oxide strip to maintain some amount of parasitic capacitance.)
Using a reverse polarity resist, the resist is developed at the emitter, and the emitter opening is defined by etching through 700A TEOS as shown in Figure 2b. The resist is then stripped and the TEOS is then used as a hardmsk to etch the 600A nitride and stop at the 100A HiPOx as shown in Figure 2c. Subsequently, the HiPOx is stripped (along with the hardmask), and an in-situ phosphorus doped emitter or an arsenic implanted emitter is formed as in Figure 2d. After the emitter poly is capped by nitride, the emitter is patterned and etched (Figure 2e). This is followed by patterning of the base region as in Figure 2f. Finally, the nitride-capped emitter poly is used as a mask for extrinsic base implant as shown in Figure 2g. In this case we use the PFET S/D implants for the extrinsic base doping rather than using a dedicated implant. This saves time and money. The advantage of non-self aligned structure is that no complicated emitter pedestal, spacer deposition and etch, Hipox conversion process is required. However, the structure becomes more sensitive to alignment (relative so the self-aligned process) as shown in Figure 2h and Figure 2i. Extrinsic base resistance must be controlled by tightening the emitter poly to emitter opening photo tolerance.(LTE and emitter poly thickness will be scaled down from generation to generation.)

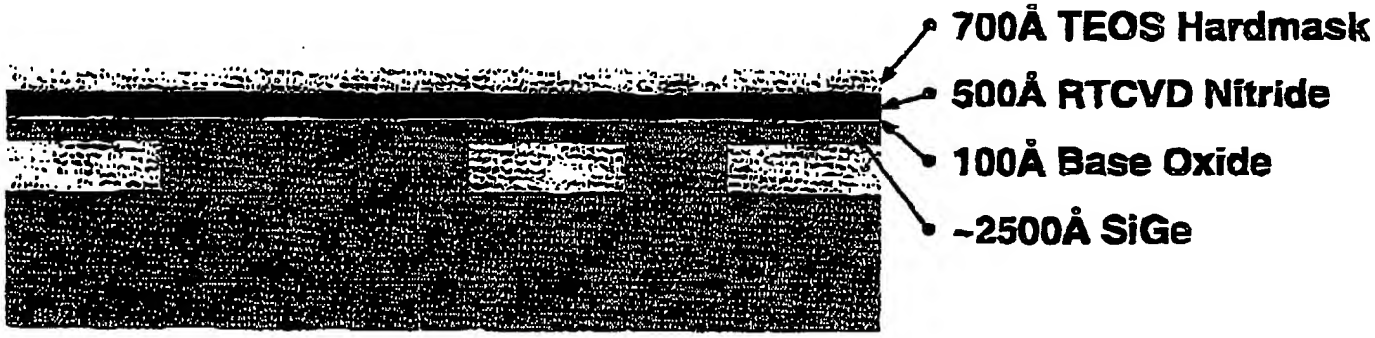


Figure 2a

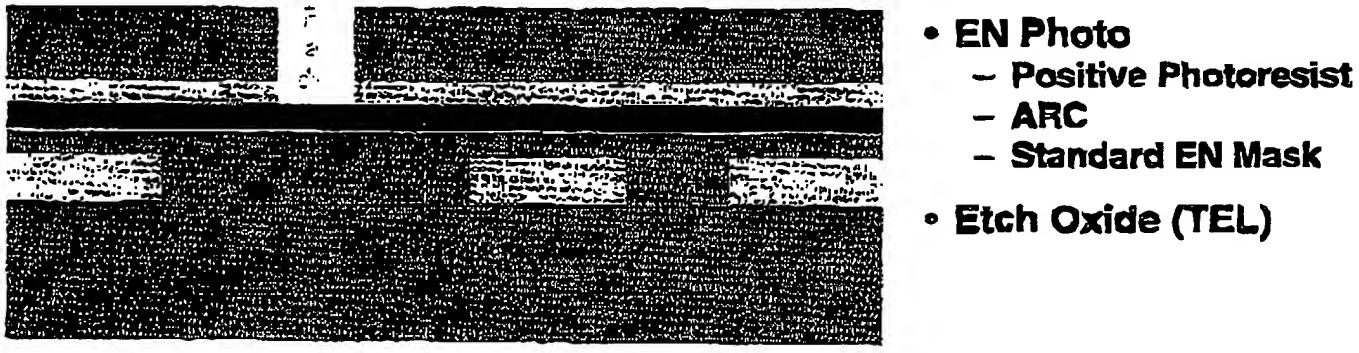
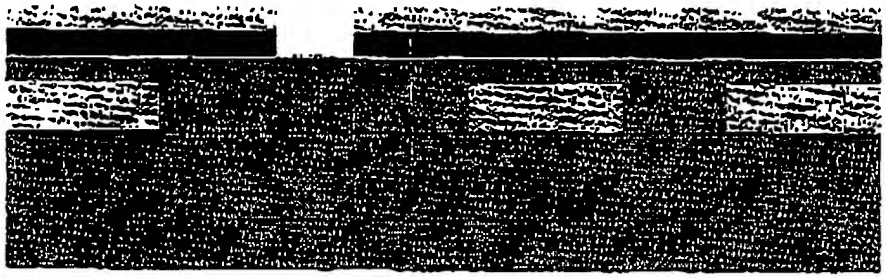
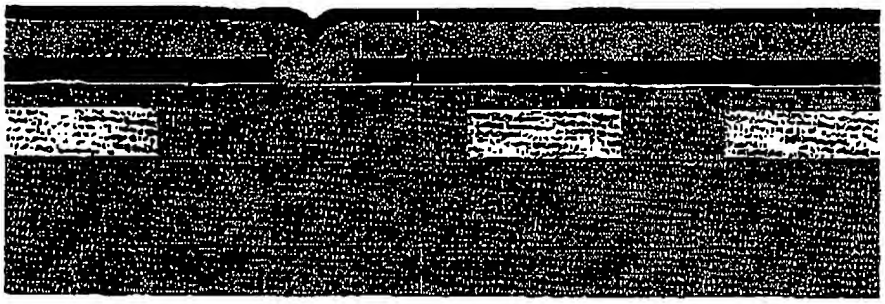


Figure 2b.



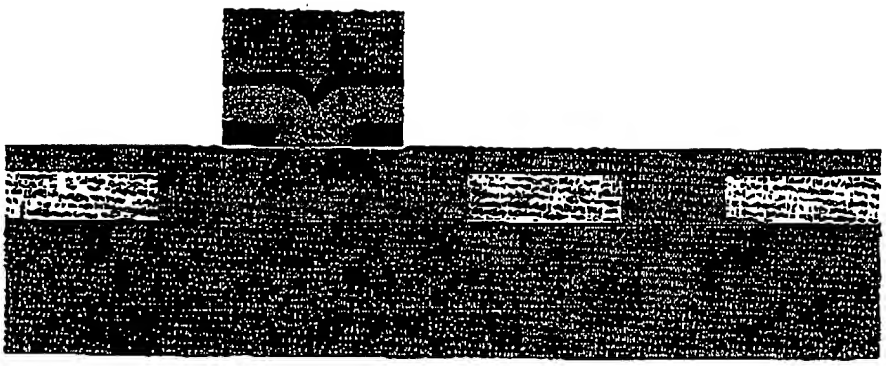
- Strip Resist
- Nitride Etch
  - Spacer chemistry
- Pedestal Implant

Figure 2c.



- RTO
- Emitter Polysilicon
- As+ Implant
- Nitride Protect

Figure 2d.



- NP Photo
- Etch Nitride
- Etch Polysilicon
- Etch Nitride

Figure 2e.

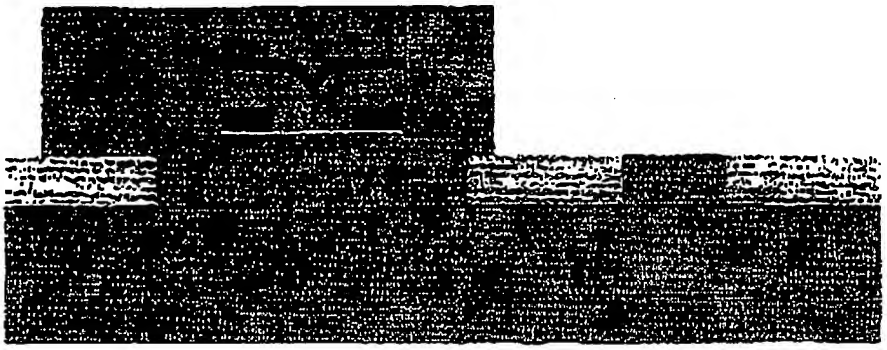


Figure 2f.

- **Base Etch Stopping on STI**

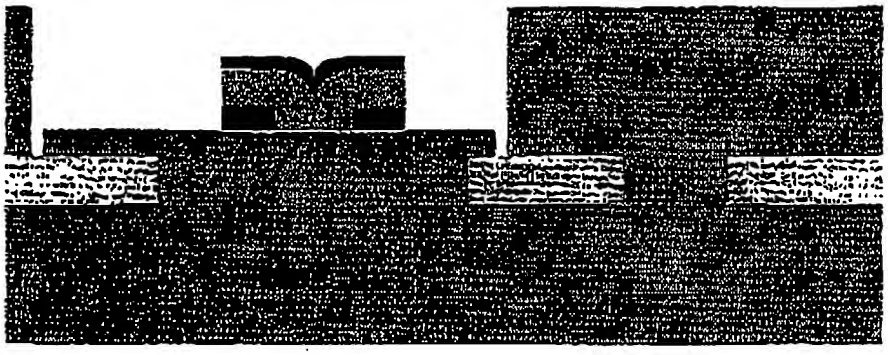


Figure 2g.

- **BN Photo**
- **Extrinsic Base Implant**
  - **FET S/D (BN)**

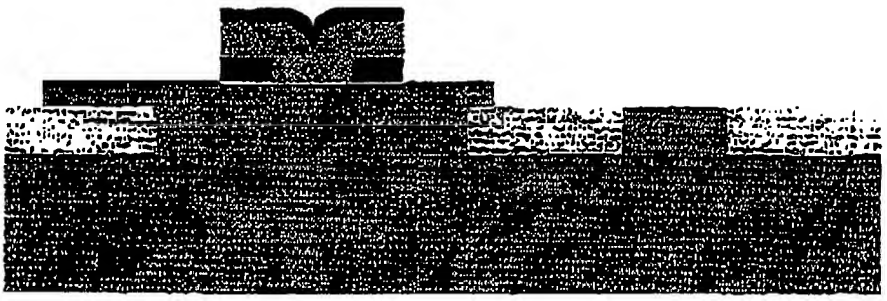


Figure 2h.

- **Perfectly aligned emitter polysilicon (NP) to emitter opening (EN) photo**

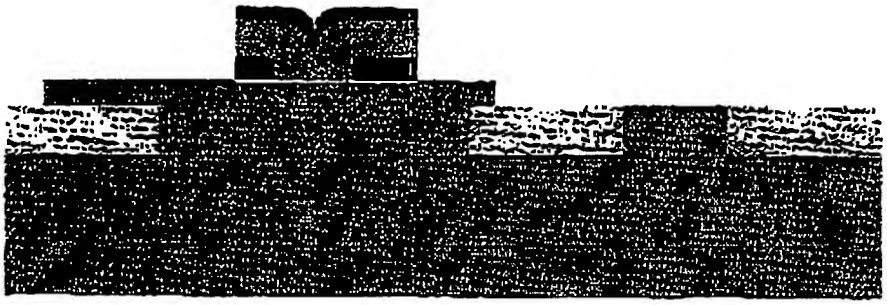


Figure 2i

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.

***Critical Questions (Questions 1 - 7 must be answered)**

Question 1 On what date was the invention workable? 04/05/2000 Please format the date as MM/DD/YYYY. Workable means i.e. when you know that your design will solve the problem.

Question 2 Is there any planned or actual publication or disclosure of your invention to anyone outside IBM?	○ Yes ● No
If yes, Enter the name of each publication or patent and the date published below. Publication/Patent: Date Published or Issued:	
Are you aware of any publications, products or patents that relate to this invention?	○ Yes ● No
If yes, Enter the name of each publication or patent and the date published below. Publication/Patent: Date Published or Issued:	

Question 3 Has the subject matter of the invention or a product incorporating the invention been sold, used internally in manufacturing, announced for sale, or included in a proposal?	○ Yes ● No
Is a sale, use in manufacturing, product announcement, or proposal planned?	○ Yes ● No
If Yes, identify the product if known and indicate the date of planned date of sale, announcement, or proposal and to whom the sale, announcement or proposal has been or will be made. Product Version/Release:	

FIS8-2000-0337 A Non-Self Aligned SiGe Heterojunction Bipolar Transistor (HBT) - continued

Code Name:
Date:
To Whom:
If more than one, use cut and paste and append as necessary in the field provided.

Question 4
Was the subject matter of your invention or a product incorporating your invention used in public e.g., outside IBM or in the presence of non-IBMers?
○ Yes ● No ○
If Yes, give a date. Please format the date as MM/DD/YYYY.

Question 5
Have you ever discussed your invention with others not employed at IBM?
○ Yes ● No
If yes, identify individuals and date discussed. Fill in the text area with the following information, the names of the individuals, the employer, date discussed, under CDA, and CDA #.

Question 6
Was the invention, in any way, started or developed under a government contract or project?
○ Yes ● No ○ Not sure
If Yes, enter the contract number.

Question 7
Was the invention made in the course of any alliance, joint development or other contract activities?
○ Yes ● No ○ Not Sure
If Yes, enter the following: Name of Alliance, Contractor or Joint Developer
Contract ID number
Relationship contact name
Relationship contact E-mail
Relationship contact phone

Question 8
Have you submitted, or are you aware of, any related disclosure submission?
○ Yes ● No
If Yes, please provide the title and docket or disclosure number below.

Question 9
What type of companies do you expect to compete with inventions of this type? Check all that apply.
- ☐ Manufacturers of enterprise servers
- ☐ Manufacturers of entry servers
- ☐ Manufacturers of workstations
- ☐ Manufacturers of PC's
- ☐ Non-computer manufacturers
- ☐ Developers of operating systems
- ☐ Developers of networking software
- ☐ Developers of application software
- ☐ Integrated solution providers
- ☐ Service providers
- ☒ Other (Please specify below)

mixed signal semiconductor companies

Patent Value Tool (Optional - this may be used by the inventor and attorney to assist with the evalua

(The Patent Value tool can be used by you or the evaluation team to determine the potential licensing value of your invention.)

The **Patent Value Tool** has not yet been used to calculate a score.

Post Disclosure Text & Drawings
Enter any additional information relating to this disclosure below:

(Form Revised 12/17/97)